# Changes to Commands and Properties

## Command Changes

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| --- | --- |
| **Command Name** | **Comment** |
| add\_output\_reg\_across\_rtl\_group | Name change. Previous name was add\_output\_reg\_across\_rtlgroup |
| show\_project | New command to print the project name |
| set\_clock\_domain\_sync\_depth | New command to set the synchronizer depth of a clock domain |
| add\_ram\_group | New command to group LLC’s that work as RAM (scratchpad) |
| del\_ram\_group | New command to delete RAM groups |
| list\_ram\_group | New command to list the added RAM groups |
| map | This command has been deprecated |
| tune\_route | This command has been deprecated |
| tune\_links | This command has been deprecated |

## Default Property Changes

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| --- | --- | --- |
| **Property Name** | **Default Value** | **Comment** |
| msg\_peak\_bw | 6.4 | This property has been deprecated |
| msg\_peak\_rate | 0.1 | This property has been deprecated |
| peak\_multiplier | 1 | New property to specify the default multiplier to calculate peak rate/bw from average rate/bw when the peak rate/bw is not specified |
| sync\_input\_register | no | New default property to enable or disable input registering at the bridge when there is no clock crossing at the bridge. |
| synchronizer\_depth | 2 | New property to specify the default value of synchronizer depth for all clock domains. |
| axi4m\_logical\_processors | 1 | New property to specify the default number of logical processors supported by the master bridge |
| axi4m\_exclusive\_support | Yes | New property to specify if a master has AXI exclusive support by default |
| sysc\_enable | no | Enable generation of SystemC LT model **(Special License needed)** |
| read\_burstiness | 1 | The default value for this property has been changed from 3 to 1 |

## Mesh Property Changes

|  |  |  |
| --- | --- | --- |
| **Property Name** | **Default Value** | **Comment** |
| compact\_regbus\_address\_space | Yes | Default value of this property has changed from No to Yes |
| extra\_bandwidth\_provisioning | 0 | Default value of this property has changed from 25 to 0 |
| sys\_r\_user\_bits\_per\_byte | -1 | New property to specify the default for the system R user width per byte. |
| sys\_r\_user\_width | -1 | New property to specify the default for the system R user width. |
| sys\_b\_user\_width | -1 | New property to specify the default for the system B user width |
| sys\_ar\_user\_width | -1 | New property to specify the default for the system AR user width |
| sys\_axi4\_aw\_aid\_width | -1 | New property to specify the default for the system AXI4 AW AID width. |
| sys\_mst\_id\_width | -1 | New property to specify the default for the system master ID width |
| sys\_aw\_user\_width | -1 | New property to specify the default for the system AW user width. |
| sys\_axi4\_addr\_width | -1 | New property to specify the default for the system AXI4 address width. |
| sys\_axi4\_ar\_aid\_width | -1 | New property to specify the default for the system AXI4 AR AID width. |
| sys\_w\_user\_bits\_per\_byte | -1 | New property to specify the default for the system W user width per byte. |
| stats\_level | High | New property to specify the default level of statistics collection in NocStudio performance simulator |
| errorcheck\_granularity | 502 | New property to specify the default upper limit of error check granularity **(Special license needed)** |

## Bridge Property Changes

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| --- | --- |
| **Property Name** | **Comment** |
| axi4s\_logical\_id\_enb | New property that indicates whether logical ID is enabled for read and write requests to a slave bridge |
| sync\_input\_register | New property that enables input registering at the bridge when there is no clock crossing at the bridge |
| acem\_dvm\_support | New property that enabled ACE masters to have connections to the DVM block |
| axi4m\_logical\_processors | New property to specify the number of logical processors supported by the master bridge |
| axi4m\_exclusive\_support | New property to specify if a master has AXI exclusive support |
| axi4m\_llc\_allocation\_class | Name change. Previous name was llc\_allocation\_class |

## Host Property Changes

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| --- | --- |
| **Property Name** | **Comment** |
| llc\_class\_write\_allocate | New property to specify how write allocation is controlled for each of the LLC classes. |
| llc\_class\_read\_allocate\_use\_arcache | New property to specify whether read allocation for each LLC class is controlled by the ARCACHE bits |
| llc\_class\_read\_allocate | New property to specify how read allocation is controlled for each of the LLC classes. |
| llc\_class\_write\_allocate\_use\_awcache | New property to specify whether write allocation for each LLC class is controlled by the AWCACHE bits. |
| llc\_second\_slave\_port\_connect | New property to specify which master connects to the second LLC slave port (if it exists) |
| llc\_slave\_port2\_read\_max\_outstanding | New property to specify the number of outstanding read requests the second LLC slave port can support from all sources. |
| llc\_slave\_port2\_write\_max\_outstanding | New property to specify the number of outstanding write requests the second LLC slave port can support from all sources |
| llc\_class0\_alloc\_waygroups | New property to specify which waygroups can be accessed by class 0 of the LLC |
| llc\_class1\_alloc\_waygroups | New property to specify which waygroups can be accessed by class 1 of the LLC |
| llc\_class2\_alloc\_waygroups | New property to specify which waygroups can be accessed by class 2 of the LLC |
| llc\_class3\_alloc\_waygroups | New property to specify which waygroups can be accessed by class 3 of the LLC |
| llc\_class4\_alloc\_waygroups | New property to specify which waygroups can be accessed by class 4 of the LLC |
| llc\_class5\_alloc\_waygroups | New property to specify which waygroups can be accessed by class 5 of the LLC |
| llc\_class6\_alloc\_waygroups | New property to specify which waygroups can be accessed by class 6 of the LLC |
| llc\_class7\_alloc\_waygroups | New property to specify which waygroups can be accessed by class 7 of the LLC |

## Interface Property Changes

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| --- | --- |
| **Property Name** | **Comment** |
| internal\_pipeline | New property to decide the type of registering between switch and protocol side for each host interface. One of these options can be enabled to remove timing paths between switch and protocol processing logic. |

## Link Property Changes

None

## Router Property Changes

None

## VC Property Changes

None